

REMARKS

Reconsideration of this application is requested. Claims 18, 20, 23, 31, 33 and 41 are pending. The other claims are or were previously cancelled.

The objections to the specification and drawings have been overcome by amending claims 18 and 49 in the manner suggested in the Action at page 3. Similarly, the objections to claims 18, 46 and 49 have been overcome by making the amendments suggested in the action. The amendments to these claims were not made to overcome a prior art rejection or a section 112 rejection.

The rejection of claims 40 (cancelled) and 41 (which now depends on claim 18) as being anticipated by Yasui (US Patent 5,248,963) is traversed and moot in view of the cancellation of claim 40 and the change in the dependency of claim 41. In view of the lack of an anticipation rejection of its independent claim 18, the anticipation rejection of claim 41 should be withdrawn.

The rejection of claims 18, 20, 23, 31, 33 and 45 to 49 for obviousness over Yasui in view of Hayashi (US Patent 5,313,282) is traversed for the reasons stated above for claims 18 and 49.

Independent claims 18 and 49 recite an LCD erasing device that applies a signal to the electrodes for the pixels after the LCD power is turned off. In particular, claim 18 recites that a "source enable signal" is applied "at a selecting level during the certain period [which is a period following power being turned off, and the selecting level] is

inputted into said source driver circuit so that said pixel electrode and said opposing electrode receive an OFF voltage that turns OFF a liquid crystal." See, e.g., appln. pp. 39-49. Similarly, claim 49 recites that the erasing means "applies rectangular wave signals, identical in terms of phase and potential, respectively into said pixel electrode and said opposing electrode during the certain period" which follows the power source being turned off. *Id.*

Yasui discloses supplying a common potential to both a display electrode 12a and a counter electrode 12b within a time (T) after the power is turned OFF (see column 6, lines 3 to 6). Yasui discloses that pixel data (D) is set to a logic "o" to clear the display. Yasui, col. 3, lns. 59-61. The pixel data is loaded into a shift register and then applied to the pixels. Yasui does not disclose a feature in which a "source enable signal" is inputted to the source driver control circuit during a predetermined period after the power source is turned OFF.

Unlike Yasui, claim 18 herein recites that a source enable signal is inputted to the source driver control circuit at a "selection level" during the predetermined period after the power source is turned OFF. Such use of the source enable signal does not complicate the circuit arrangement and allows application to the pixel electrode and the opposing electrode, a voltage for turning OFF the liquid crystal. because Yasui teaches display erasing by means other than a source enable signal, it teaches away from the invention recited in claim 18

Claims 45 and 49 recite "rectangular wave signals" being applied by the LCD erasing means. In contrast to claim 49, Yasui discloses applying a constant common (ground) potential to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF (see column 6, lines 3 to 6). Yasui (column 1, line 52) states "common potential EG (zero volt", the "common potential EG" is the ground potential. Therefore, Yasui teaches that a ground potential EG is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF. Yasui (column 5, line 6, to column 6, line 1) describes that "[t]he source bus driver 16b is arranged so that the potential as its output terminal goes to the common potential EG at substantially the same time as the operating voltages E_1 , E_2 and E_3 drop to the common potential".

The Action incorrectly characterizes Yasui as disclosing at column 3, line 58 to column 4, line 16, that a voltage \underline{E}_2 equal to the voltage (E_2) of the common electrodes 12b is applied to the source buses 14t through 14₁ through 14_n so as to clear the display image within the duration T. Yasui (column 1, lines 45 to 60) states that the \underline{E}_2 is a DC voltage (corresponding to the central "E" among "E"s in D in Figure 2), which satisfies:

$$E_2 = (E_1 + E_3)/2$$

$$E_1 > 0 > E_2 > E_3$$

This description in Yasui indicates that the negative DC voltage E_2 is supplied to both the display electrode 12a and the counter electrode 12b within the time T after the power is turned OFF. Yasui discloses that a ground potential EG, or the DC voltage E_2

equal thereto is supplied to both the display electrode 12a and the counter electrode 12b when clearing the display image

Accordingly, Yasui does not disclose the rectangular wave signals, recited in claim 49, that are identical in terms of phase and potential, respectively into said pixel electrode and the opposing electrode.

Hayashi discloses that a TV receiver is turned OFF by shutting off a power supply to each section of the TV receiver from a power supply circuit 21 based on a signal from a remote controller 20. Hayashi turns off power to a display of a television, but retains power to other portions of the TV in order to allow for a video recording to be made of a received TV signal after the display has be shut off. Hayashi teaches nothing about erasing an image from the display before turning OFF power to the display.

The combination of Yasui and Hayashi would not have rendered obvious the claimed inventions. In particular, Hayashi does not suggest that Yasui's technique for display erasing should be discarded in favor of the technique claimed here.

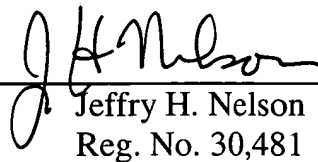
All claims are in good condition for allowance. If any small matter remains outstanding, the Examiner is requested to telephone the undersigned. Prompt reconsideration and allowance of this application is requested.

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Respectfully submitted,

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